What is claimed is:

1. An analysis method for a semiconductor device, comprising:

measuring electrical characteristics of a plurality of test element groups fabricated on a semiconductor substrate;

classifying the test element groups into a first test element group category where a systematic failure has not occurred and a second test element group category where the systematic failure has occurred based on the electrical characteristics;

creating a first comparison Mahalanobis reference space using first parameters of the test element groups in the first test element group category from among parameters of the test element groups expressed as numerical values;

calculating a first comparison Mahalanobis distance of the first parameters and a second comparison Mahalanobis distance of second parameters of the test element groups in the second test element group category by using the first comparison Mahalanobis reference space; and

comparing the first and second comparison Mahalanobis distances.

2. The analysis method of claim 1, wherein when no

significant difference between the calculated first and second comparison Mahalanobis distances is determined, the method repeats loop processing which includes:

creating a second comparison Mahalanobis reference space using the first parameters after adding another parameter expressed as a numerical value, to each of the first and second parameters;

recalculating a third comparison Mahalanobis distance of the first parameters and a fourth comparison Mahalanobis distance of the second parameters, using the second comparison Mahalanobis reference space; and

comparing the third and fourth comparison Mahalanobis distances, the loop processing being repeated until a significant difference between the third and fourth comparison Mahalanobis distances is determined.

3. The analysis method of claim 2, wherein when one of differences between the first and second comparison Mahalanobis distances, and between the third and fourth comparison Mahalanobis distances provides a significant difference, the method further comprises:

creating an orthogonal array having two levels for each of the parameters of the test element groups, a

first level of which has been used for creating a first evaluation Mahalanobis reference space, and a second level of which has not been used for creating the first evaluation Mahalanobis reference space;

creating the first evaluation Mahalanobis reference space and a second evaluation Mahalanobis reference space of the second parameters corresponding to the first and second levels based on the orthogonal array;

calculating first and second evaluation Mahalanobis distances of the second parameters by using the first and second evaluation Mahalanobis reference spaces; and

obtaining a signal to noise ratio from the first and second evaluation Mahalanobis distances as characteristic values.

4. The analysis method of claim 3, further comprising:

extracting a third parameter having a large gain of signal to noise ratio from the signal to noise ratio for each of the parameters, and

reviewing a manufacturing process which resulted in an occurrence of the systematic failure based on the third parameter.

5. The analysis method of claim 1, wherein the test

element groups include at least one of an open-short test element group to inspect open and short wiring failures and a via chain test element group connected in a chain shape by via plugs between multilevel wirings.

6. The analysis method of claim 5, wherein the parameters of the open-short test element group include at least one of a line length, a line width, a space width between lines, a wiring density including any surrounding region, a wiring coverage rate, a coordinate of the open-short test element group in a chip region, a coordinate of the chip region on the semiconductor substrate, wiring densities of the test element groups placed on an upper layer and a lower layer of the open-short test element group, and wiring coverage rates of the test element groups placed on the upper layer and the lower layer.

7. The analysis method of claim 5, wherein the parameters of the via chain test element group include at least one of a line length, a line width, a space width between lines, a wiring density including any surrounding region, a wiring coverage rate, a coordinate of the via chain test element group in the chip region, a coordinate of the chip region on the

semiconductor substrate, wiring densities of the test element groups placed on an upper layer and a lower layer of the via chain test element group, wiring coverage rates of the test element groups placed on the upper layer and the lower layer, a lower layer fringe width of a via, an upper layer fringe width of the via, a via period, a via scale, and a via opening ratio.

8. The analysis method of claim 1, wherein the first and second test element group categories are classified by using a manufacturing yield of the test element groups in the semiconductor substrate, a failure rate converted by a critical area or a via scale, and a deviation in the occurrence of a failure in a surface of the semiconductor substrate.

9. The analysis method of claim 1, wherein the test element groups are placed in the chip region of the semiconductor substrate.

10. The analysis method of claim 1, wherein the test element groups are placed in a dicing line of the semiconductor substrate.

11. An analysis system, comprising:

a failure classification module configured to

classify test element groups into a first test element group category where a systematic failure has not occurred and a second test element group category where the systematic failure has occurred based on measurement results of electrical characteristics of the test element groups; and

a statistical analysis module configured to create a first comparison Mahalanobis reference space using first parameters of the test element groups in the first test element group category from among parameters of the test element groups expressed as numerical values, and to calculate a first comparison Mahalanobis distance of the first parameters and a second comparison Mahalanobis distance of second parameters of the test element groups in the second test element group category by using the first comparison Mahalanobis reference space, so as to compare the first and second comparison Mahalanobis distances.

12. The analysis system of claim 11, wherein when no significant difference between the first and second comparison Mahalanobis distances is determined, the statistical analysis module recalculates a third comparison Mahalanobis distance of the first parameters and a fourth comparison Mahalanobis distance of the second parameters using a second

comparison Mahalanobis reference space of the first parameters which is created by loop processing, adding another parameter expressed as a numerical value to each of the first and second parameters, so as to compare the third and fourth comparison Mahalanobis distances, the loop processing repeats until a significant difference between the third and fourth comparison Mahalanobis distances is determined.

13. The analysis system of claim 11, wherein the statistical analysis module creates an orthogonal array having two levels for each of the parameters of the test element groups, a first level of which has been used for creating a first evaluation Mahalanobis reference space, and a second level of which has not been used for creating the first evaluation Mahalanobis reference space, creates the first evaluation Mahalanobis reference space and a second evaluation Mahalanobis reference space of the second parameters corresponding to the first and second levels based on the orthogonal array, calculates first and second evaluation Mahalanobis distances of the second parameters by using the first and second evaluation Mahalanobis reference spaces, and obtains a signal to noise ratio from the first and second evaluation Mahalanobis distances as characteristic values.

14. The analysis system of claim 13, further comprising a parameter extraction section configured to extract a third parameter having a large gain of signal to noise ratio from the signal to noise ratio for each of the parameters.

15. The analysis system of claim 11, further comprising a parameter storage unit configured to store data of a specification and a design layout in a specification database and a design layout database.

16. The analysis system of claim 11, further comprising a measurement information storage unit configured to store the measurement results of the electrical characteristics of the test element groups.

17. A computer program product configured to be executed by a computer, comprising:

an instruction of classifying test element groups into a first test element group category where a systematic failure has not occurred and a second test element group category where the systematic failure has occurred based on measurement results of electrical characteristics of the test element groups;

an instruction of creating a first comparison

Mahalanobis reference space using first parameters of the test element groups in the first test element group category from among parameters of the test element groups expressed as numerical values; and

an instruction of calculating a first comparison Mahalanobis distance of the first parameters and a second comparison Mahalanobis distance of second parameters of the test element groups in the second test element group category by using the first comparison Mahalanobis reference space so as to compare the first and second comparison Mahalanobis distances.

18. The computer program product of claim 17, further comprising repeating loop processing when no significant difference between the calculated first and second comparison Mahalanobis distances is determined, including:

an instruction of creating a second comparison Mahalanobis reference space using the first parameters after adding another parameter expressed as a numerical value, to each of the first and second parameters;

an instruction of recalculating a third comparison Mahalanobis distance of the first parameters and a fourth comparison Mahalanobis distance of the second parameters, using the

second comparison Mahalanobis reference space; and

an instruction of comparing the third and fourth comparison Mahalanobis distances, the loop processing being repeated until a significant difference between the third and fourth comparison Mahalanobis distances is determined.

19. The computer program product of claim 17, further comprising:

an instruction of creating an orthogonal array having two levels for each of the parameters of the test element groups, a first level of which has been used for creating a first evaluation Mahalanobis reference space, and a second level of which has not been used for creating the first evaluation Mahalanobis reference space;

an instruction of creating the first evaluation Mahalanobis reference space and a second evaluation Mahalanobis reference space of the second parameters corresponding to the first and second levels based on the orthogonal array;

an instruction of calculating first and second evaluation Mahalanobis distances of the second parameters by using the first and second evaluation

Mahalanobis reference spaces; and

an instruction of obtaining a signal to noise ratio from the first and second evaluation Mahalanobis distances as characteristic values.

20. The computer program product of claim 19, further comprising:

an instruction of extracting a third parameter having a large gain of a signal to noise ratio from the signal to noise ratio for each of the parameters; and

an instruction of reviewing a manufacturing process which resulted in an occurrence of the systematic failure based on the extracted parameter.